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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,780	10/29/2003	Tsukasa Ooishi	009683-485	6707

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EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/694,780	OOISHI, TSUKASA	
	Examiner	Art Unit	
	Gene N Auduong	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-31 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-31 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10-29-2003.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on October 29, 2003 is being considered by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-7, 9-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Ooishi (U.S. Pat. No. 5,644,250).

Regarding claim 1, Ooishi discloses a semiconductor device, comprising: an internal circuit receiving supply of an operating current VCI from a power supply node VCE (figure 2, external power supply node VCE); a current switch connected between an operating voltage source and the power supply node col. 8, lines 30+; col. 2, lines 44+); and a leakage detecting circuit for detecting whether a leakage current of the internal circuit is not greater than a reference level, the leakage detecting circuit including a reference current supply portion supplying a current of the reference level to the power supply node in an off period of the current

switch, and a voltage comparison circuit for comparing a voltage of the power supply node with a prescribed voltage in the off period (figure 15, col. 18, lines 19+; col. 2, lines 62+).

Regarding claim 2, Ooishi discloses the semiconductor device according to claim 1, wherein the reference current supply portion has a reference current adjust portion which changes the reference level stepwise in response to an adjustment designation (col. 4, lines 1-4).

Regarding claim 3, Ooishi discloses the semiconductor device according to claim 1, further comprising: an internal voltage control circuit controlling an internal voltage applied to a field effect transistor constituting the internal circuit; and an internal voltage interconnection transmitting the internal voltage; the internal voltage control circuit including an internal voltage comparison circuit comparing a voltage of the internal voltage interconnection with an object voltage, a voltage control circuit controlling the internal voltage based on a comparison result in the internal voltage comparison circuit, and a voltage adjust portion for changing the object voltage in response to an adjustment input (col. 2, lines 62+; col. 8, lines 30+; col. 18, lines 19+).

Regarding claim 4. The semiconductor device according to claim 3, wherein the adjustment input being input in a standby mode is set based on a state where the leakage current becomes not greater than the reference level at the time of an operation test (col. 2, lines 62+; col. 8, lines 30+; col. 18, lines 19+).

Regarding claim 5, Ooishi discloses the semiconductor device according to claim 3, wherein the current switch is turned off in a standby mode, and the adjustment input to the voltage adjust portion is set based on an output of the voltage comparison circuit (col. 2, lines 62+; col. 8, lines 30+; col. 18, lines 19+).

Regarding claim 6, Ooishi discloses the semiconductor device according to claim 1, wherein the internal circuit includes at least one field effect transistor (see figure 15), the semiconductor device further comprising: an internal voltage control circuit for controlling an internal voltage applied to one of source, gate, drain and substrate of the field effect transistor included in the internal circuit; and an internal voltage interconnection transmitting the internal voltage; the internal voltage control circuit including an internal voltage comparison circuit for comparing a voltage of the internal voltage interconnection with an object voltage, a voltage control circuit controlling the internal voltage based on a comparison result in the internal voltage comparison circuit, and a voltage adjust portion for changing the object voltage in response to an adjustment input (col. 2, lines 62+; col. 8, lines 30+; col. 18, lines 19+).

Regarding claim 7, Ooishi disclose the semiconductor device according to claim 6, wherein the adjustment input differs in a normal operation mode and a standby mode (col. 8, lines 62+).

Claims 9-17 and 18-31 contain the similar limitation as previously discussed in claims 1-5. Therefore, they are analyzed as previously discussed with respect to claims 1-5. It's noted that, claims 18-31 further claiming the write current lines and their routing direction in the device. Therefore, the circuit as disclosed by Ooishi would be satisfied the limitation as claimed.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ooishi (U.S. Pat. No. 5,644,250).

Regarding claim 8, Ooishi discloses the semiconductor device having all of the limitation according to claim 6. Ooishi discloses the semiconductor device having the internal voltage control circuit including an internal voltage comparison circuit comparing a voltage of the internal voltage interconnection with an object voltage, a voltage control circuit controlling the internal voltage based on a comparison result in the internal voltage comparison circuit, and a voltage adjust portion for changing the object voltage in response to an adjustment input as stated in claim 3 but does not explicitly disclose wherein the voltage adjust portion includes a voltage-divider circuit which divides a voltage difference between the internal voltage and a prescribed voltage with a divide ratio in accordance with the adjustment input, and the internal voltage comparison circuit compares the divided voltage output from the voltage-divider circuit with a fixed reference voltage. However, the voltage-divider circuit is known and normally being used in the device to divide the internal voltage to a predetermined voltage level to meet the requirement voltage range of a specific elements in the device such as reference voltage generator 922 shown in figure 2. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the conventionally used voltage-divider circuit in Ooishi's device to divide the internal voltage to a predetermined voltage level for a specific elements in the circuit so that those elements can be operate in a stable state and prolong the life of those elements.

Double Patenting

7. Claims 1-5 and 9-17 of this application conflict with claims 1-5 and 9-17 of Application No. 10/410,206. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

8. Claims 6-8 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 6-8 of copending Application No. 10/410,206. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are claiming the same scope of the invention.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (571) 272-1773.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
November 30, 2004

Gene N Auduong
Primary Examiner
Art Unit 2818